PATENT
Docket No.: 492322017600

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Tetsuro ASANO *et al.*

Serial No.: 10/772,585

Filing Date: February 6, 2004

For: SEMICONDUCTOR DEVICE

Examiner: Not yet assigned

Group Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Pursuant to 37 CFR 1.97 and 1.98, Applicants submit for consideration in this application the documents listed on the attached Form PTO-1449. Copies of the documents are also submitted herewith. The Examiner is requested to make these documents of record.

This Information Disclosure Statement is being submitted within three months of the application filing date or before mailing of a first Office Action on the merits; accordingly, no fee or separate requirements are required.

Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement under 37 CFR 1.97 and 1.98 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional

information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

In the unlikely event that the transmittal form is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing 492322017600.

Dated: July 6, 2004

Respectfully submitted,

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The semiconductor device according to the present invention includes a conductive substrate; a semi-insulating crystal layer grown on the conductive substrate; an electronic circuit formed in the semi-insulating crystal layer; an input/output terminal and a power supply terminal which are connected to the electronic circuit; a first conductive region formed between the electronic circuit and the input/output terminal; and a second conductive region formed between the electronic circuit and the power supply terminal, which are monolithically integrated such that the withstanding voltages between the first and second conductive regions and the conductive substrate are less than the withstanding voltage of the electronic circuit.

Another semiconductor device according to the present invention includes a conductive substrate; a semi-insulating crystal layer grown on the conductive substrate; an active element formed in the semi-insulating crystal layer; at least first and second terminals formed in the active element; a first conductive region connected to the first terminal of the active element; and a second conductive region formed between the active element and the second terminal, which are monolithically integrated such that the withstanding voltages between the first and second conductive regions and the conductive substrate are less than the withstanding voltage of the active element.

Therefore, surge voltages added to the electronic circuit are absorbed within the chip and prevented from entering the electronic circuit, so that the electronic circuit may not be damaged and operate normally. Furthermore, there is no need for attaching an external surge absorption circuit to the integrated circuit. The semiconductor device can be constituted as a monolithic integrated circuit.

Moreover, since it is possible to afford the resistance to surge to the active element itself constituting the integrated circuit, there is no need for taking measures against the surge for the sake of the outside of the integrated circuit.

Thus, a monolithically integrated semiconductor device having the resistance to the surge can be constituted.

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number 492322017600	Application Number 10/772,585
Applicant: Tetsuro ASANO et al.	
Filing Date February 6, 2004	Group Art Unit 2812
Mailing Date July 6, 2004	

U.S. PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES	Translation NO
	1.	3/1/95	8-236549	Japan			abstract	
	2.	12/16/88	2723936	Japan			abstract	

OTHER DOCUMENTS *(including author, title, Date, Pertinent Pages, Etc.)*

Examiner Initials	Ref. No.	Title

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.